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A Network-On Chip Architecture for Optimization of Area and Power with Reconfigurable Topology on Cyclone II Specific Device

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ABSTRACT : *The Network-on-Chip (NoC) architecture enables the network topology to be reconfigured.This enables a general System-on-Chip (SoC) platform, which is currently running on the chip. The topology is configured using area- efficient topology and so it is optimised design*

KEYWORDS: *SOC, NOC, Area and power efficient, CMOS sensor application*

I. INTRODUCTION

Every new CMOS technology generation enables the design of larger and more complex systems on a single integrated circuit. The increasing complexity also means that design, test and production costs reach levels where large volumes must be produced for a chip to be feasible. The time it takes to get a new product to the market (time-to market) thereby also increases. This trend seems to make ASICs infeasible for the main bulk of applications the development time will simply be too long. For many applications a more general System-on-Chip (SoC) platform chip could be a viable solution. Such a SoC platform would contain many different IP-Blocks including RAMs, CPUs, DSPs, IOs, FPGAs and other coarse and fine grained programmable IP-Blocks. The communication is provided by means of a flexible communication infrastructure in the form of a Network-on-Chip (NoC). This allows the same SoC platform to be used in a wide range of different applications and thereby increases the production volume. As the same SoC platform is to be used for many different applications, the NoC must be able to support a wide range of bandwidth and Quality-of-Service (QoS) requirements. The requirements of the applications can be very different, and the NoC must therefore be very flexible. Currently, the only way to provide such flexibility is to employ a large packet-switched NoC with an over-engineered total bandwidth capacity. Such a NoC would take a significant part of the SoCs silicon area and only a fraction of its capacity is utilized by a given application. The topology switches are implemented using physical circuit-switching as found in FPGAs, to minimize the power consumption and area overhead. The motivation for inserting a configurable layer below existing NoC architectures is that physical circuit switching is far more efficient than intelligent, complex packet-switching which therefore must be avoided when possible. The communication requirement for the application is therefore used to configure a logical topology that minimizes the amount of packet-switching.

II HETEROGENEOUS PHYSICAL ARCHITECTURE:

In this architecture we are using routers and topology switches separately as well as combined also taking for network nodes and so the architecture is complex

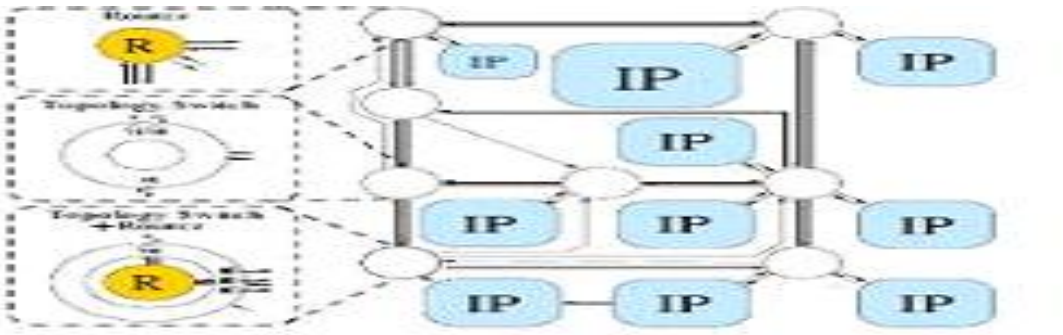


Figure 1 : Example of a complex, heterogeneous, physical architecture

Network nodes can contain a router, a topology switch, or both. Several IP-cores can be connected to the same network node, several link scan exist between network nodes, and IP-blocks can be directly connected.

The architecture is not restricted to a specific router. The only requirement is that the link width, including wires for flow-control, matches the ports on the router. In principle the communication protocol is defined by the routers and the topology switches and links act as passive circuit-switched interconnects. This means that the architecture can be used in combination with any existing router. The routers can contain Virtual Channels (VC), Quality of-Service (QoS) implementations such as TDM, queuing buffers, and can be implemented using synchronous or asynchronous circuit techniques.

III CMOS SENSOR APPLICATION AS BENCHMARK

Input can be used as real-time raw video streams from the CMOS sensor board in which we can do image capturing, video processing from basic images. Tools using for this process is Quartus II, Sopc builder, NiosII

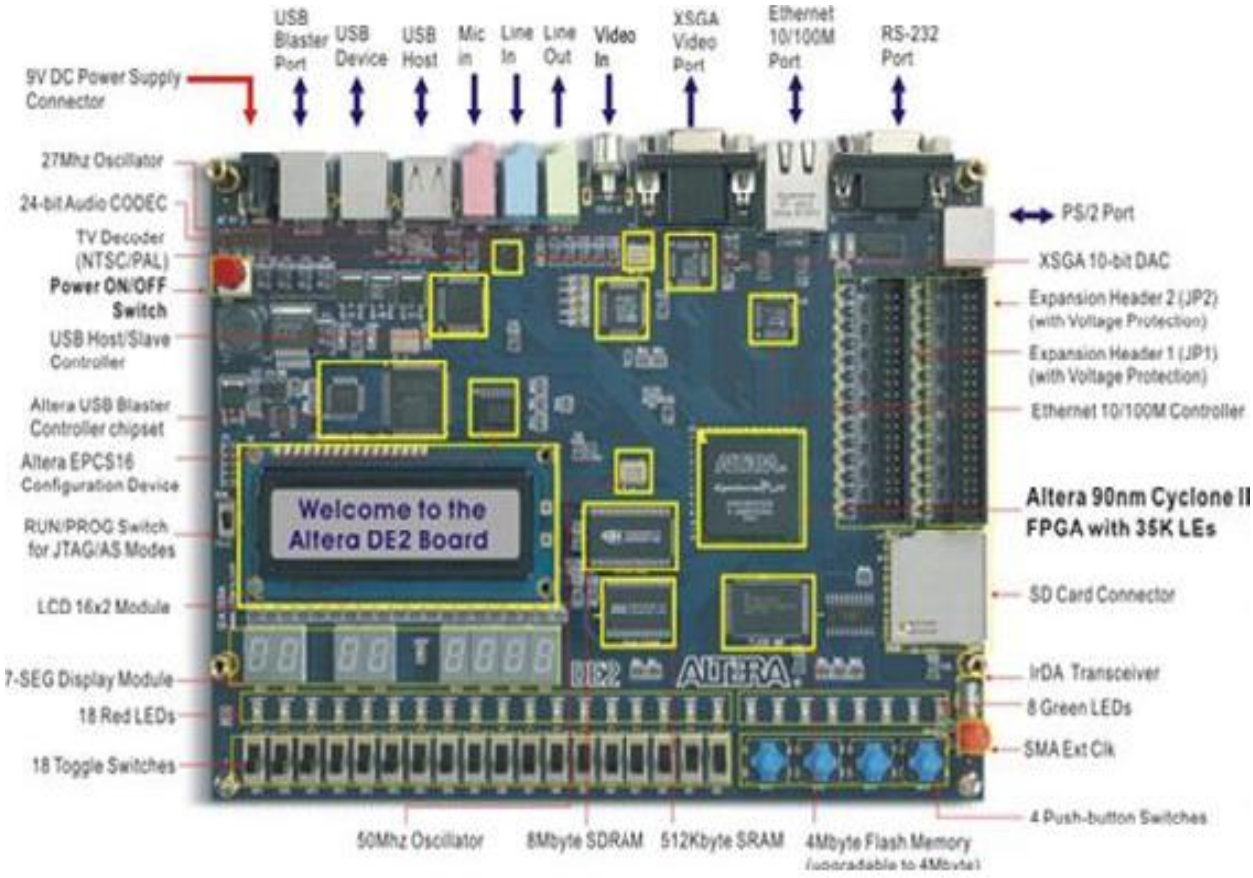
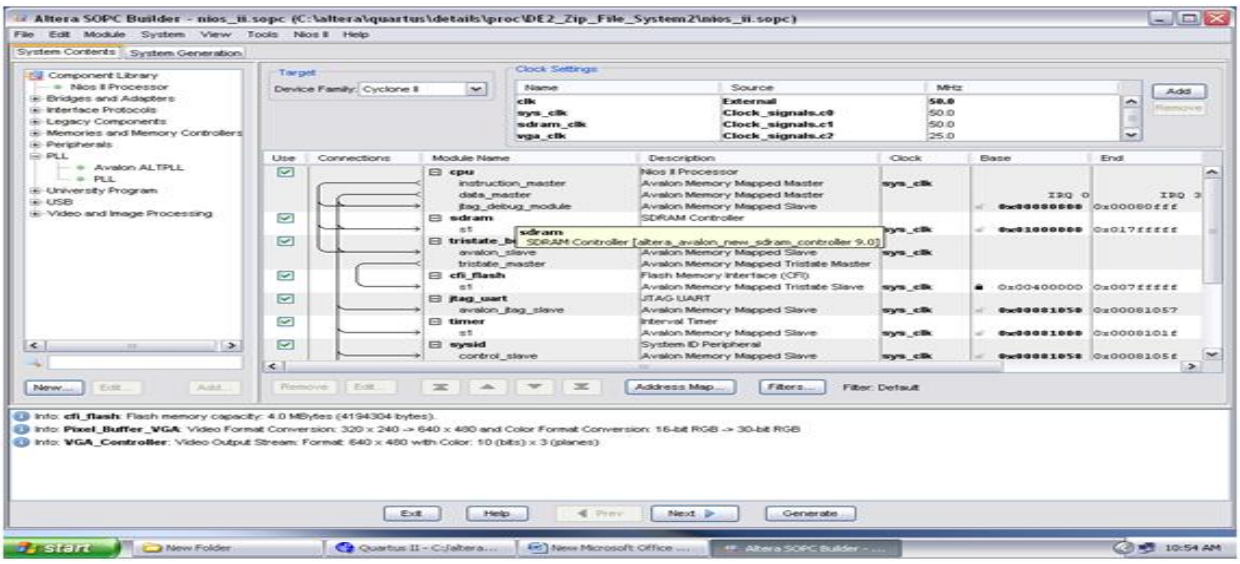


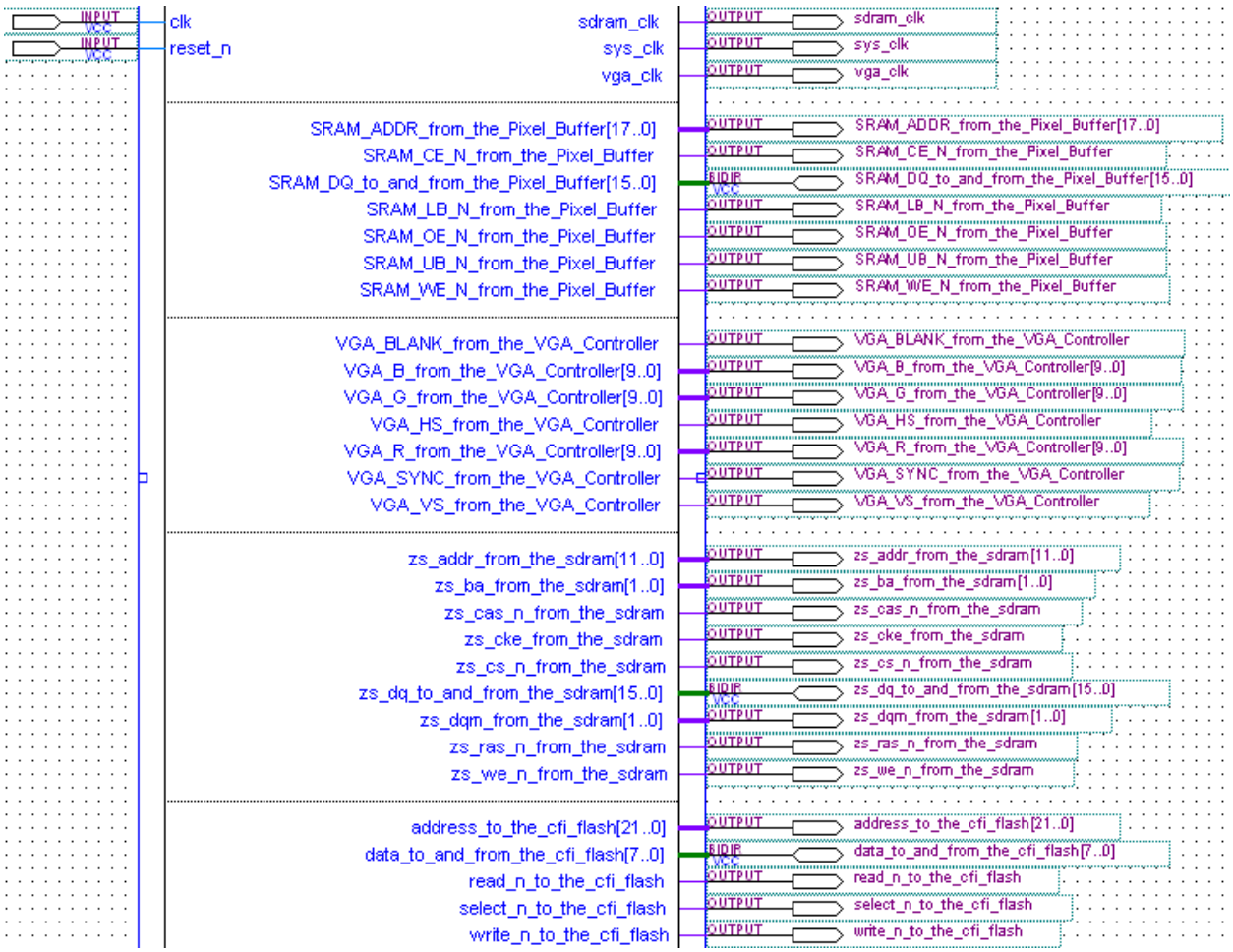
Figure 2: Overview of cyclone II DE2 BOARD

This is a basic cyclone II DE2 board for video processing which can be interfaced with extra CMOS SENSOR daughter card. The basic kit contains RS232 serial port and video input port and video output serial ports. So that implementation of video processing is possible without a LCD touch panel display in the base kit Through Synopsys tools (.i.e., Design vision, prime time) we can estimate optimised area and power of our design but can't be implemented in fpgas before chip fabrication. So in order to check our designs before fabrication we are going to quartus II and nios II software tools for estimations of optimised area and power as well as we can implement on FPGAS

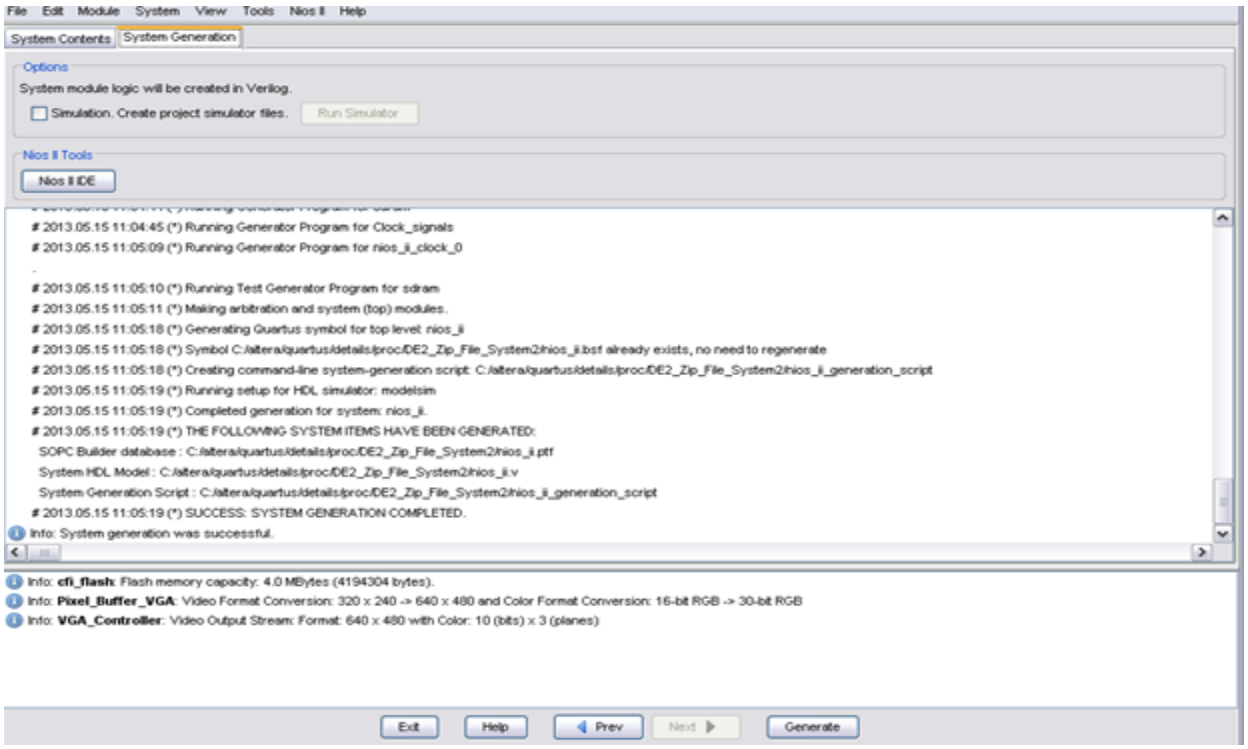
VOPD application building



VOPD Schematic



Result for SoC Generation



SoC Implementation results for Area of specific device

Flow Summary

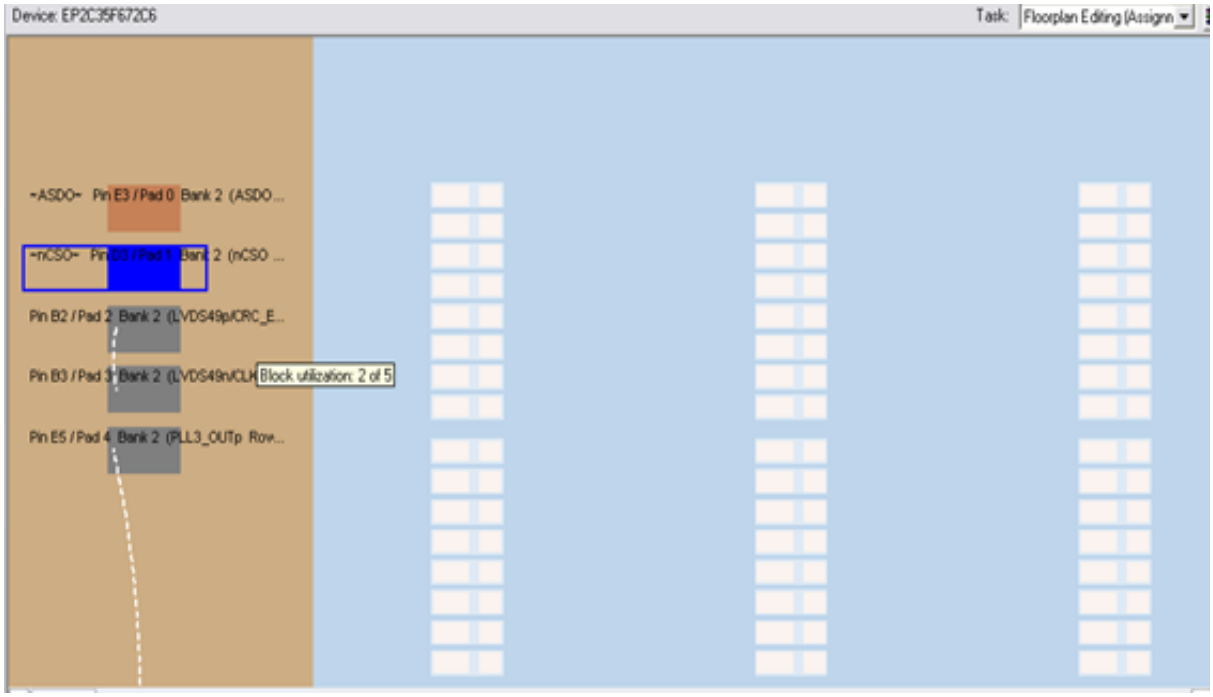
Flow Status	Successful - Fri Nov 22 06:42:31 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	0 / 33,216 (0 %)
Total combinational functions	0 / 33,216 (0 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	426 / 475 (90 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

Power estimated for SoC Implementation of specific device

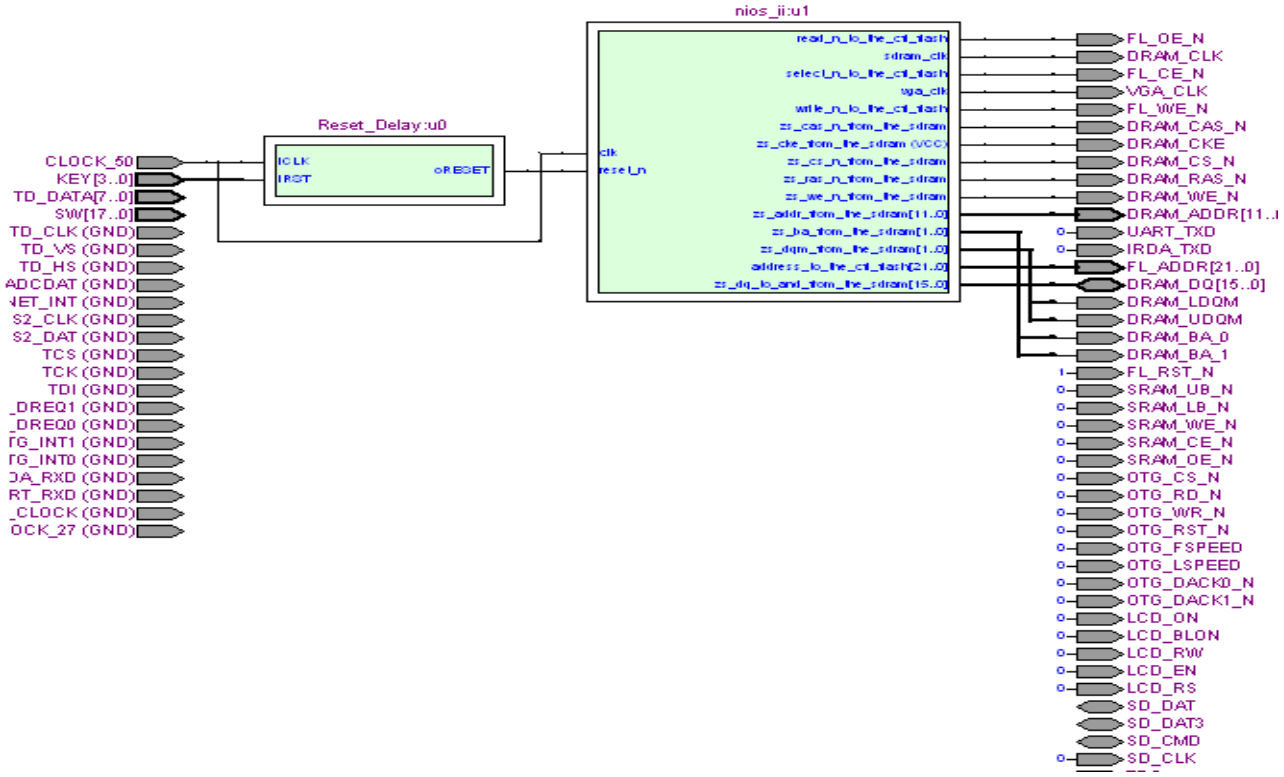
PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Fri Nov 22 07:02:01 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	160.87 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	80.09 mW
I/O Thermal Power Dissipation	80.78 mW
Power Estimation Confidence	High: user provided sufficient toggle rate data

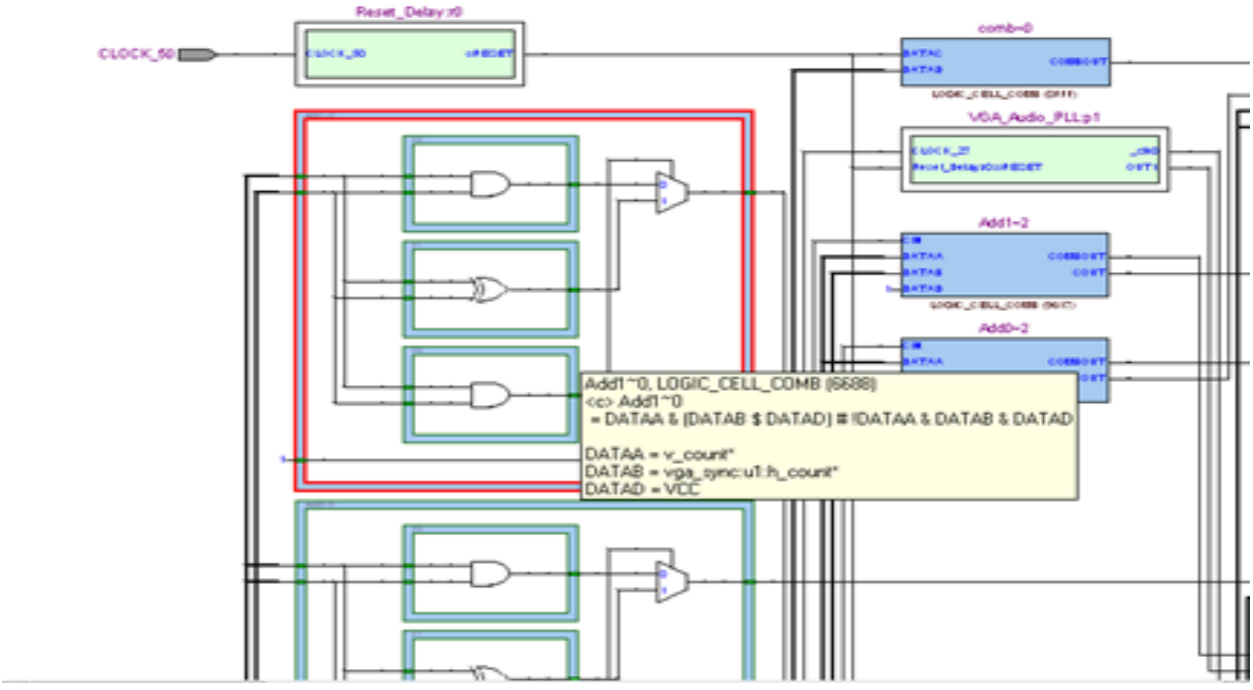
Chip planner



RTL schematic



Technology post mapping



NoC implementation results for area of specific device

Flow Summary

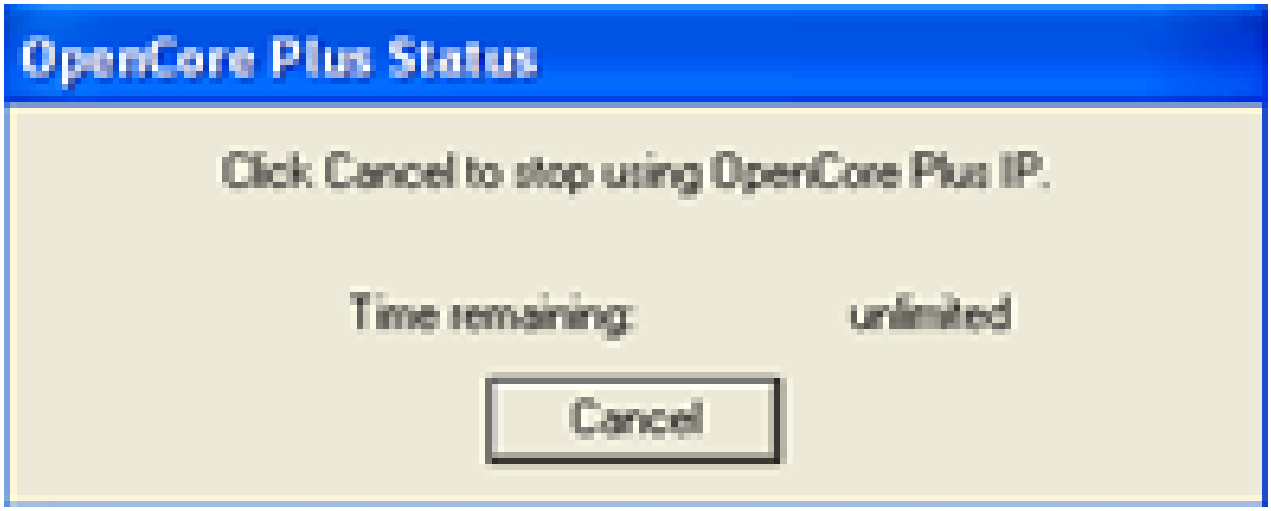
Flow Status	Successful - Fri Nov 22 06:21:56 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	4,624 / 33,216 (14 %)
Total combinational functions	4,142 / 33,216 (12 %)
Dedicated logic registers	2,813 / 33,216 (8 %)
Total registers	2930
Total pins	426 / 475 (90 %)
Total virtual pins	0
Total memory bits	75,136 / 483,840 (16 %)
Embedded Multiplier 9-bit elements	4 / 70 (6 %)
Total PLLs	1 / 4 (25 %)

Power estimation for NoC implementation of specific device

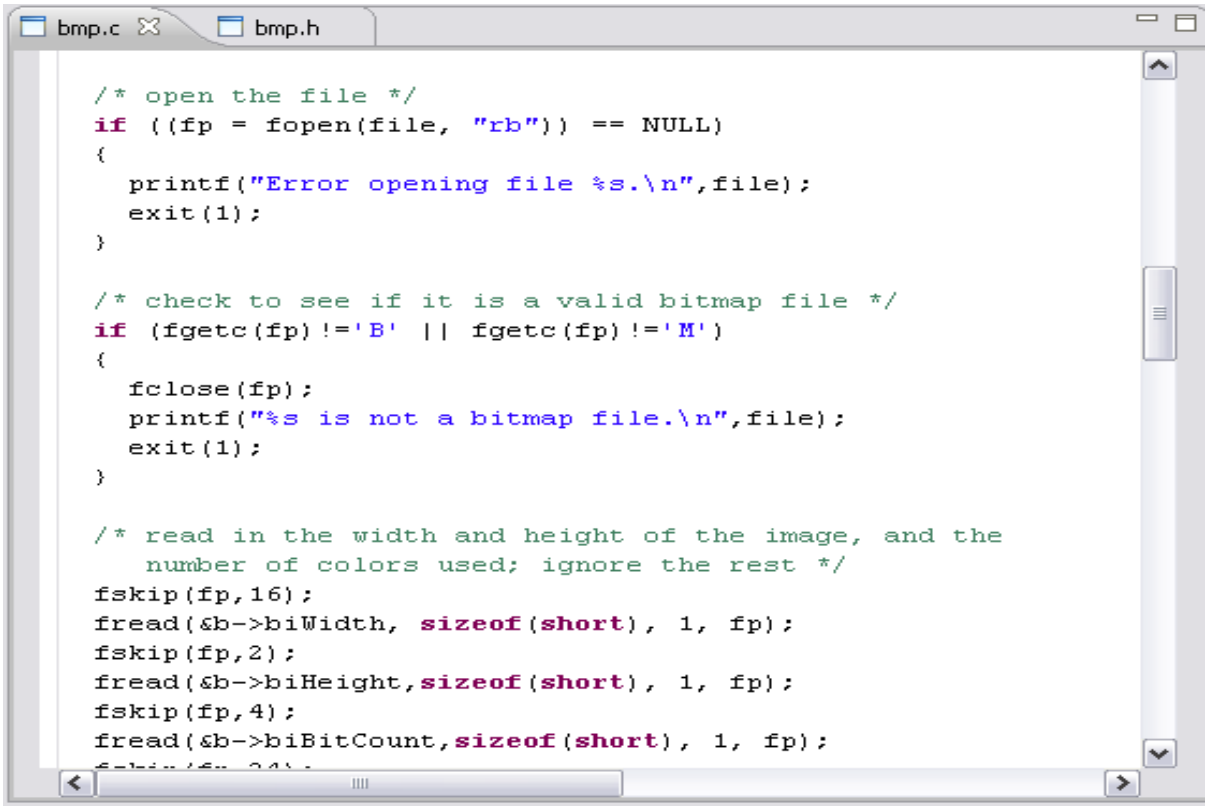
PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Fri Nov 22 06:38:02 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	DE2_Zip_File_System2
Top-level Entity Name	DE2_Zip_File_System2
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	161.18 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	80.09 mW
I/O Thermal Power Dissipation	81.09 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Wizard display while connecting to niosII processor



Building embedded designs using nios II wizard



Implementation of NoC using nios II

bmp.c bmp.h

```
#ifndef BMP_H_
#define BMP_H_

typedef struct {              /* the structure for a bitmap. *
  short biWidth;
  short biHeight;
  short biBitCount;
  char *bicolor_palatte;
  short *data;
} bitmap_struct;

void load_bmp(char *file, bitmap_struct *b);

void fskip(FILE *fp, int num_bytes);

unsigned short bmp_color_convert24_16(char* color24);


#endif /*BMP_H_*/
```

IV CONCLUSION AND FEATURE WORK

We are using CMOS SENSOR BOARD for this application in which we are giving digital video as real time input and also we can capture image from the real time video processing.

This can be basic idea to further research to video conferencing, multimedia applications, and IP surveillance cameras

REFERENCE

[1] V.Ravikiran, Dr. M. Devaraju, "A Network-on Chip Architecture for Optimization of area and power with Reconfigurable Topology on FPGAs", International Journal of Engineering Science, Volume 2 Issue 8, PP.52-59, 2013

[2] P. Magarshack and P. G. Paulin, "System-on-chip beyond the nanometer wall," in DAC 03: Proceeding of the 40th conference on Design automation. NewYork, NY, USA: ACM Press2003,

[3] W. J. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks," in Design Automation, 2001

[4] G. de Micheli and L. Benini, "Networks on chip: A new paradigm for systems on chip design," 2002

[5] W. J. Dally, "'enabling technology for on-chip interconnection networks' keynote presentation at 'the 1st acm/ieee international symposium on networks-on-chip2007

[6] A. Banerjee**,** R. Mullins, and **S**. Moore, "A power and energy exploration of network-on-chip architectures," 1st international symposium, 2007.

[7**]** M. Modarressi, "A reconfigurable topology for NoCs," Tech. Rep. TR-HPCAN10-2, 2010.

[8] D**.** Bertozzi, A. Jalabert, S. Murali, R. Tamahankar**,S.**Stergiou**,** L. Benini, and G. De Micheli, "NoC synthesis flow for customized domain specific multiprocessor systems-on-chip," IEEE Trans. Parallel Distrib. Syst., vol. 16, no. 2, pp. 113–129, Feb. 2005.

[9] T. Bjerregaard and J. Sparsø, "A router architecture for connection-oriented service guarantees in the mango clockless network-on-chip," in Proc. Design Automation and Test in Europe (DATE'05), ACM sigda, 2005, pp. 1226–1231.